

# DDR2 SDRAM SODIMM

MT16HTS25664H – 2GB<sup>1</sup>

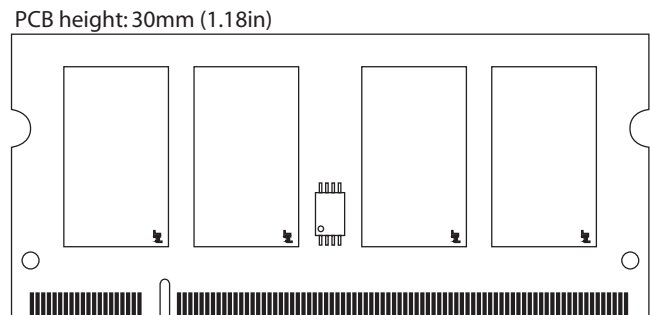
MT16HTS51264H – 4GB

For component specifications, refer to Micron's Web site: [www.micron.com](http://www.micron.com)

## Features

- 200-pin, small outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- 2GB (256 Meg x 64) and 4GB (512 Meg x 64)
- VDD = VDDQ = +1.8V
- VDDSPD = +1.7V to +3.6V
- JEDEC standard 1.8V I/O (SSTL\_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 t<sub>CK</sub>
- Programmable burst lengths (BL) 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank, TwinDie™ (2COB) DRAM devices

Figure 1: 200-Pin SODIMM (MO-224 R/C D)



## Options

- Operating temperature<sup>2</sup>
  - Commercial (0°C ≤ T<sub>A</sub> ≤ +70°C)
  - Industrial (-40°C ≤ T<sub>A</sub> ≤ +85°C)
- Package
  - 200-pin DIMM (Pb-free)
- Frequency/CAS latency
  - 3.0ns @ CL = 5 (DDR2-667)
  - 3.75ns @ CL = 4 (DDR2-533)
  - 5.0ns @ CL = 3 (DDR2-400)<sup>3</sup>

## Marking

None  
I  
Y  
-667  
-53E  
-40E

Notes: 1. End of life.

2. Contact Micron for industrial temperature module offerings.

3. Not recommended for new designs.

Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) |        |        | t <sub>RCD</sub> (ns) | t <sub>RP</sub> (ns) | t <sub>RC</sub> (ns) |
|-------------|-----------------------|------------------|--------|--------|-----------------------|----------------------|----------------------|
|             |                       | CL = 5           | CL = 4 | CL = 3 |                       |                      |                      |
| -667        | PC2-5300              | 667              | 533    | 400    | 15                    | 15                   | 55                   |
| -53E        | PC2-4200              | -                | 533    | 400    | 15                    | 15                   | 55                   |
| -40E        | PC2-3200              | -                | 400    | 400    | 15                    | 15                   | 55                   |



**Table 2: Addressing**

| Parameter            | 2GB                       | 4GB                       |
|----------------------|---------------------------|---------------------------|
| Refresh count        | 8K                        | 8K                        |
| Row address          | 16K (A0–A13)              | 32K (A0–A14)              |
| Device bank address  | 8 (BA0–BA2)               | 8 (BA0–BA2)               |
| Device configuration | 2Gb TwinDie (128 Meg x 8) | 4Gb TwinDie (256 Meg x 8) |
| Column address       | 1K (A0–A9)                | 1K (A0–A9)                |
| Module rank address  | 2 (S0#, S1#)              | 2 (S0#, S1#)              |

**Table 3: Part Numbers and Timing Parameters – 2GB**

Base device: MT47H256M8THJ,<sup>1</sup> 2Gb TwinDie DDR2 SDRAM

| Part Number <sup>2</sup> | Module Density | Configuration | Module Bandwidth | Memory Clock/<br>Data Rate | Clock Cycles<br>(CL- <sup>t</sup> RCD- <sup>t</sup> RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|---|
| MT16HTS25664HY-667__     | 2GB            | 256 Meg x 64  | 5.3 GB/s         | 3.0ns/667 MT/s             | 5-5-5   |
| MT16HTS25664HY-53E__     | 2GB            | 256 Meg x 64  | 4.3 GB/s         | 3.75ns/533 MT/s            | 4-4-4   |
| MT16HTS25664HY-40E__     | 2GB            | 256 Meg x 64  | 3.2 GB/s         | 5.0ns/400 MT/s             | 3-3-3   |

**Table 4: Part Numbers and Timing Parameters – 4GB**

Base device: MT47H512M8THM,<sup>1</sup> 4Gb TwinDie DDR2 SDRAM

| Part Number <sup>2</sup> | Module Density | Configuration | Module Bandwidth | Memory Clock/<br>Data Rate | Clock Cycles<br>(CL- <sup>t</sup> RCD- <sup>t</sup> RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|---|
| MT16HTS51264HY-667__     | 4GB            | 512 Meg x 64  | 5.3 GB/s         | 3.0ns/667 MT/s             | 5-5-5   |
| MT16HTS51264HY-53E__     | 4GB            | 512 Meg x 64  | 4.3 GB/s         | 3.75ns/533 MT/s            | 4-4-4   |

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
  2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes.  
Example: MT16HTS51264HY-667A1.



## Pin Assignments and Descriptions

Table 5: Pin Assignments

| 200-Pin SODIMM Front |        |     |        |     |        |     |        | 200-Pin SODIMM Back |        |                 |        |     |        |     |        |
|----------------------|--------|-----|--------|-----|--------|-----|--------|---------------------|--------|-----------------|--------|-----|--------|-----|--------|
| Pin                  | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin                 | Symbol | Pin             | Symbol | Pin | Symbol | Pin | Symbol |
| 1                    | VREF   | 51  | DQS2   | 101 | A1     | 151 | DQ42   | 2                   | Vss    | 52              | DM2    | 102 | A0     | 152 | DQ46   |
| 3                    | Vss    | 53  | Vss    | 103 | VDD    | 153 | DQ43   | 4                   | DQ4    | 54              | Vss    | 104 | VDD    | 154 | DQ47   |
| 5                    | DQ0    | 55  | DQ18   | 105 | A10    | 155 | Vss    | 6                   | DQ5    | 56              | DQ22   | 106 | BA1    | 156 | Vss    |
| 7                    | DQ1    | 57  | DQ19   | 107 | BA0    | 157 | DQ48   | 8                   | Vss    | 58              | DQ23   | 108 | RAS#   | 158 | DQ52   |
| 9                    | Vss    | 59  | Vss    | 109 | WE#    | 159 | DQ49   | 10                  | DM0    | 60              | Vss    | 110 | SO#    | 160 | DQ53   |
| 11                   | DQS0#  | 61  | DQ24   | 111 | VDD    | 161 | Vss    | 12                  | Vss    | 62              | DQ28   | 112 | VDD    | 162 | Vss    |
| 13                   | DQS0   | 63  | DQ25   | 113 | CAS#   | 163 | NC     | 14                  | DQ6    | 64              | DQ29   | 114 | ODT0   | 164 | CK1    |
| 15                   | Vss    | 65  | Vss    | 115 | S1#    | 165 | Vss    | 16                  | DQ7    | 66              | Vss    | 116 | A13    | 166 | CK1#   |
| 17                   | DQ2    | 67  | DM3    | 117 | VDD    | 167 | DQS6#  | 18                  | Vss    | 68              | DQS3#  | 118 | VDD    | 168 | Vss    |
| 19                   | DQ3    | 69  | NC     | 119 | ODT1   | 169 | DQS6   | 20                  | DQ12   | 70              | DQS3   | 120 | NC     | 170 | DM6    |
| 21                   | Vss    | 71  | Vss    | 121 | Vss    | 171 | Vss    | 22                  | DQ13   | 72              | Vss    | 122 | Vss    | 172 | Vss    |
| 23                   | DQ8    | 73  | DQ26   | 123 | DQ32   | 173 | DQ50   | 24                  | Vss    | 74              | DQ30   | 124 | DQ36   | 174 | DQ54   |
| 25                   | DQ9    | 75  | DQ27   | 125 | DQ33   | 175 | DQ51   | 26                  | DM1    | 76              | DQ31   | 126 | DQ37   | 176 | DQ55   |
| 27                   | Vss    | 77  | Vss    | 127 | Vss    | 177 | Vss    | 28                  | Vss    | 78              | Vss    | 128 | Vss    | 178 | Vss    |
| 29                   | DQS1#  | 79  | CKE0   | 129 | DQS4#  | 179 | DQ56   | 30                  | CK0    | 80              | CKE1   | 130 | DM4    | 180 | DQ60   |
| 31                   | DQS1   | 81  | VDD    | 131 | DQS4   | 181 | DQ57   | 32                  | CK0#   | 82              | VDD    | 132 | Vss    | 182 | DQ61   |
| 33                   | Vss    | 83  | NC     | 133 | Vss    | 183 | Vss    | 34                  | Vss    | 84              | NC     | 134 | DQ38   | 184 | Vss    |
| 35                   | DQ10   | 85  | BA2    | 135 | DQ34   | 185 | DM7    | 36                  | DQ14   | 86 <sup>1</sup> | NC/A14 | 136 | DQ39   | 186 | DQS7#  |
| 37                   | DQ11   | 87  | VDD    | 137 | DQ35   | 187 | Vss    | 38                  | DQ15   | 88              | VDD    | 138 | Vss    | 188 | DQS7   |
| 39                   | Vss    | 89  | A12    | 139 | Vss    | 189 | DQ58   | 40                  | Vss    | 90              | A11    | 140 | DQ44   | 190 | Vss    |
| 41                   | Vss    | 91  | A9     | 141 | DQ40   | 191 | DQ59   | 42                  | Vss    | 92              | A7     | 142 | DQ45   | 192 | DQ62   |
| 43                   | DQ16   | 93  | A8     | 143 | DQ41   | 193 | Vss    | 44                  | DQ20   | 94              | A6     | 144 | Vss    | 194 | DQ63   |
| 45                   | DQ17   | 95  | VDD    | 145 | Vss    | 195 | SDA    | 46                  | DQ21   | 96              | VDD    | 146 | DQS5#  | 196 | Vss    |
| 47                   | Vss    | 97  | A5     | 147 | DM5    | 197 | SCL    | 48                  | Vss    | 98              | A4     | 148 | DQS5   | 198 | SA0    |
| 49                   | DQS2#  | 99  | A3     | 149 | Vss    | 199 | VDDSPD | 50                  | NC     | 100             | A2     | 150 | Vss    | 200 | SA1    |

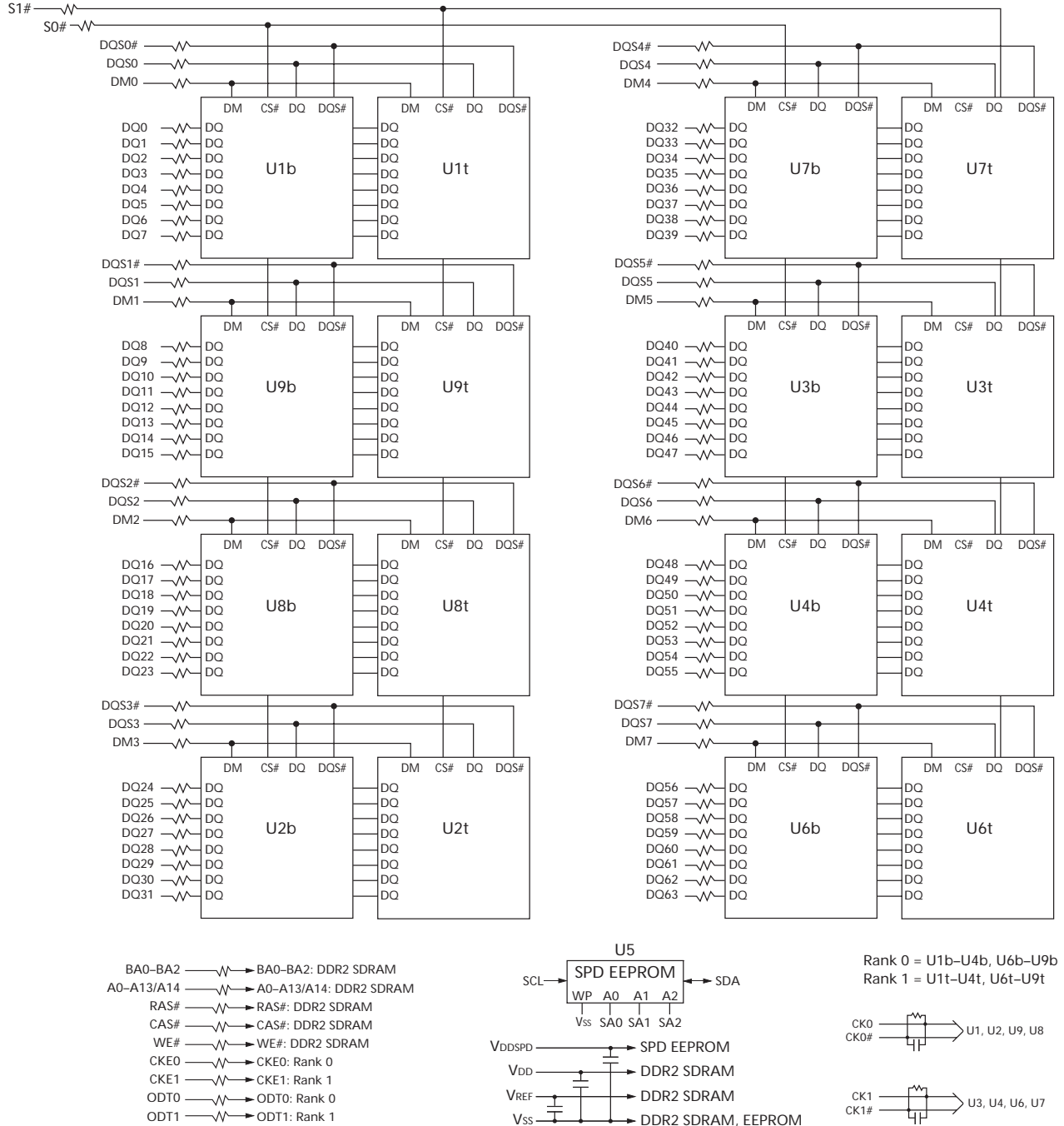
Notes: 1. Pin 86 is NC for 2GB and A14 for 4GB.

**Table 6: Pin Descriptions**

| Symbol                    | Type            | Description  |
|---------------------------|-----------------|--|
| A0–A14                    | Input (SSTL_18) | <b>Address inputs:</b> Provide the row address for ACTIVE commands and the column address, and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A0–A13 (2GB) and A0–A14 (4GB). |
| BA0–BA2                   | Input (SSTL_18) | <b>Bank address inputs:</b> BA0–BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.  |
| CK0, CK0#<br>CK1, CK1#    | Input (SSTL_18) | <b>Clock:</b> CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#.   |
| CKE0, CKE1                | Input (SSTL_18) | <b>Clock enable:</b> CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.  |
| DM0–DM7                   | Input (SSTL_18) | <b>Data input mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.  |
| ODT0, ODT1                | Input (SSTL_18) | <b>On-die termination:</b> ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.   |
| RAS#, CAS#,<br>WE#        | Input (SSTL_18) | <b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.   |
| S0#, S1#                  | Input (SSTL_18) | <b>Chip select:</b> S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.   |
| SA0–SA1                   | Input (SSTL_18) | <b>Presence-detect address inputs:</b> These pins are used to configure the presence-detect devices.   |
| SCL                       | Input (SSTL_18) | <b>Serial clock for presence-detect:</b> SCL is used to synchronize the presence-detect data transfer to and from the module.  |
| DQ0–DQ63                  | I/O (SSTL_18)   | <b>Data input/output:</b> Bidirectional data bus.  |
| DQS0–DQS7,<br>DQS0#–DQS7# | I/O (SSTL_18)   | <b>Data strobe:</b> Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.   |
| SDA                       | I/O (SSTL_18)   | <b>Serial presence-detect data:</b> SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.  |
| VDD                       | Supply          | <b>Power supply:</b> +1.8 ±0.1V.   |
| VDDSPD                    | Supply          | <b>Serial EEPROM positive power supply:</b> +1.7V to +3.6V.  |
| VREF                      | Supply          | SSTL_18 reference voltage (VDD/2).   |
| VSS                       | Supply          | Ground.  |
| NC                        | –               | <b>No connect:</b> These pins are not connected on the module.   |

## Functional Block Diagram

Figure 2: Functional Block Diagram



## General Description

The MT16HTS25664H and MT16HTS51264H DDR2 SDRAM modules are high-speed, CMOS, dynamic random access 2GB and 4GB memory modules organized in a x64 configuration. These modules use 2Gb and 4Gb TwinDie DDR2 SDRAM devices with eight internal banks.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single  $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I<sup>2</sup>C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (1:0), which provide four unique DIMM/EEPROM addresses. Write protect (WP) is pulled down to VSS on the module, permanently disabling hardware write protect.

## Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 7: Absolute Maximum Ratings**

| Symbol          | Parameter   | Min                               | Max  | Units   |             |
|-----------------|---|-----------------------------------|------|---------|-------------|
| VDD             | VDD supply voltage relative to VSS  | -1.0                              | +2.3 | V       |             |
| VIN, VOUT       | Voltage on any pin relative to VSS  | -0.5                              | +2.3 | V       |             |
| II              | Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$ ; VREF input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V) | Address inputs<br>RAS#, CAS#, WE# | -80  | +80     | $\mu A$     |
|                 |   | S#, CKE, ODT, CK,<br>CK#          | -40  | +40     |             |
|                 |   | DM                                | -10  | +10     |             |
| Ioz             | Output leakage current; $0V \leq V_{OUT}$ ; DQ and ODT are disabled   | -10                               | +10  | $\mu A$ |             |
| IVREF           | VREF leakage current; VREF = valid VREF level   | -32                               | +32  | $\mu A$ |             |
| TA              | Module ambient operating temperature  | Commercial                        | 0    | +70     | $^{\circ}C$ |
|                 |   | Industrial                        | -40  | +85     | $^{\circ}C$ |
| TC <sup>1</sup> | DDR2 SDRAM component case operating temperature <sup>2</sup>  | Commercial                        | 0    | +85     | $^{\circ}C$ |
|                 |   | Industrial                        | -40  | +95     | $^{\circ}C$ |

- Notes: 1. The refresh rate is required to double when  $85^{\circ}C < T_C \leq 95^{\circ}C$ .  
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

## Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

## AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

**Table 8: Module and Component Speed Grades**

| Module Speed Grade | Component Speed Grade |
|--------------------|-----------------------|
| -667               | -3                    |
| -53E               | -37E                  |
| -40E               | -53E                  |

**Table 9: DDR2 IDD Specifications and Conditions – 2GB**

Values are shown for the MT47H256M8THJ DDR2 SDRAM only and are computed from values specified in the 2Gb TwinDie (256 Meg x 8) component data sheet

| Parameter/Condition   | Symbol                      | -667   | -53E  | -40E  | Units |    |
|---|-----------------------------|--------|-------|-------|-------|----|
| <b>Operating one bank active-precharge current:</b> $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} MIN (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching   | IDD0                        | 776    | 656   | 656   | mA    |    |
| <b>Operating one bank active-read-precharge current:</b> $I_{OUT} = 0mA$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} MIN (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W   | IDD1                        | 896    | 856   | 816   | mA    |    |
| <b>Precharge power-down current:</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating   | IDD2P                       | 112    | 112   | 112   | mA    |    |
| <b>Precharge quiet standby current:</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating   | IDD2Q                       | 376    | 376   | 336   | mA    |    |
| <b>Precharge standby current:</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching   | IDD2N                       | 416    | 416   | 376   | mA    |    |
| <b>Active power-down current:</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating  | Fast PDN exit<br>MR[12] = 0 | IDD3Pf | 296   | 296   | 296   | mA |
|   | Slow PDN exit<br>MR[12] = 1 | IDD3Ps | 136   | 136   | 136   | mA |
| <b>Active standby current:</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} MAX (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching   | IDD3N                       | 536    | 456   | 416   | mA    |    |
| <b>Operating burst write current:</b> All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} MAX (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching  | IDD4W                       | 1,176  | 1,096 | 936   | mA    |    |
| <b>Operating burst read current:</b> All device banks open; Continuous burst read; $I_{OUT} = 0mA$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} MAX (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching   | IDD4R                       | 1,176  | 1,096 | 936   | mA    |    |
| <b>Burst refresh current:</b> $t_{CK} = t_{CK} (IDD)$ ; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching  | IDD5                        | 1,816  | 1,776 | 1,736 | mA    |    |
| <b>Self refresh current:</b> CK and CK# at 0V; $CKE \leq 0.2V$ ; Other control and address bus inputs are floating; Data bus inputs are floating  | IDD6                        | 112    | 112   | 112   | mA    |    |
| <b>Operating bank interleave read current:</b> All device banks interleaving reads; $I_{OUT} = 0mA$ ; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$ ; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RRD} = t_{RRD} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | IDD7                        | 2,336  | 2,256 | 2,176 | mA    |    |



**Table 10: DDR2 IDD Specifications and Conditions – 4GB**

Values are shown for the MT47H512M8THM DDR2 SDRAM only and are computed from values specified in the 4Gb TwinDie (512 Meg x 8) component data sheet

| Parameter/Condition  | Symbol                      | -667   | -53E  | Units |    |
|--|-----------------------------|--------|-------|-------|----|
| <b>Operating one bank active-precharge current:</b> $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching  | IDD0                        | 904    | 824   | mA    |    |
| <b>Operating one bank active-read-precharge current:</b> $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MIN} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W   | IDD1                        | 1,264  | 944   | mA    |    |
| <b>Precharge power-down current:</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating  | IDD2P                       | 128    | 128   | mA    |    |
| <b>Precharge quiet standby current:</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating  | IDD2Q                       | 504    | 424   | mA    |    |
| <b>Precharge standby current:</b> All device banks idle; $t_{CK} = t_{CK} (IDD)$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching  | IDD2N                       | 584    | 504   | mA    |    |
| <b>Active power-down current:</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating   | Fast PDN exit<br>MR[12] = 0 | IDD3Pf | 384   | 344   | mA |
|  | Slow PDN exit<br>MR[12] = 1 | IDD3Ps | 144   | 144   | mA |
| <b>Active standby current:</b> All device banks open; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching  | IDD3N                       | 544    | 464   | mA    |    |
| <b>Operating burst write current:</b> All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching   | IDD4W                       | 1,304  | 1,144 | mA    |    |
| <b>Operating burst read current:</b> All device banks open; Continuous burst reads; $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$ , $t_{RAS} = t_{RAS} \text{ MAX} (IDD)$ , $t_{RP} = t_{RP} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching  | IDD4R                       | 1,464  | 1,304 | mA    |    |
| <b>Burst refresh current:</b> $t_{CK} = t_{CK} (IDD)$ ; Refresh command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching   | IDD5                        | 2,344  | 2,184 | mA    |    |
| <b>Self refresh current:</b> CK and CK# at 0V; CKE $\leq 0.2\text{V}$ ; Other control and address bus inputs are floating; Data bus inputs are floating  | IDD6                        | 128    | 128   | mA    |    |
| <b>Operating bank interleave read current:</b> All device banks interleaving reads; $I_{OUT} = 0\text{mA}$ ; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$ ; $t_{CK} = t_{CK} (IDD)$ , $t_{RC} = t_{RC} (IDD)$ , $t_{RRD} = t_{RRD} (IDD)$ , $t_{RCD} = t_{RCD} (IDD)$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | IDD7                        | 2,824  | 2,464 | mA    |    |

## Serial Presence-Detect

**Table 11: Serial Presence-Detect EEPROM DC Operating Conditions**

| Parameter/Condition  | Symbol                      | Min          | Max          | Units |
|--|-----------------------------|--------------|--------------|-------|
| Supply voltage   | VDDSPD                      | 1.7          | 3.6          | V     |
| Input high voltage: Logic 1; All inputs                    | V <sub>IH</sub>             | VDDSPD × 0.7 | VDDSPD + 0.5 | V     |
| Input low voltage: Logic 0; All inputs                     | V <sub>IL</sub>             | -0.6         | VDDSPD × 0.3 | V     |
| Output low voltage: I <sub>OUT</sub> = 3mA                 | V <sub>OL</sub>             | -            | 0.4          | V     |
| Input leakage current: V <sub>IN</sub> = GND to VDD        | I <sub>LI</sub>             | 0.10         | 3.0          | μA    |
| Output leakage current: V <sub>OUT</sub> = GND to VDD      | I <sub>LO</sub>             | 0.05         | 3.0          | μA    |
| Standby current  | I <sub>SB</sub>             | 1.6          | 4.0          | μA    |
| Power supply current, READ: SCL clock frequency = 100 kHz  | I <sub>CC<sub>R</sub></sub> | 0.4          | 1.0          | mA    |
| Power supply current, WRITE: SCL clock frequency = 100 kHz | I <sub>CC<sub>W</sub></sub> | 2.0          | 3.0          | mA    |

**Table 12: Serial Presence-Detect EEPROM AC Operating Conditions**

| Parameter/Condition   | Symbol              | Min | Max | Units | Notes |
|---|---------------------|-----|-----|-------|-------|
| SCL LOW to SDA data-out valid                               | t <sup>AA</sup>     | 0.2 | 0.9 | μs    | 1     |
| Time the bus must be free before a new transition can start | t <sup>BUF</sup>    | 1.3 | -   | μs    |       |
| Data-out hold time  | t <sup>DH</sup>     | 200 | -   | ns    |       |
| SDA and SCL fall time                                       | t <sup>F</sup>      | -   | 300 | ns    | 2     |
| Data-in hold time   | t <sup>HD:DAT</sup> | 0   | -   | μs    |       |
| Start condition hold time                                   | t <sup>HD:STA</sup> | 0.6 | -   | μs    |       |
| Clock HIGH period   | t <sup>HIGH</sup>   | 0.6 | -   | μs    |       |
| Noise suppression time constant at SCL, SDA inputs          | t <sup>I</sup>      | -   | 50  | ns    |       |
| Clock LOW period  | t <sup>LOW</sup>    | 1.3 | -   | μs    |       |
| SDA and SCL rise time                                       | t <sup>R</sup>      | -   | 0.3 | μs    | 2     |
| SCL clock frequency   | f <sup>SCL</sup>    | -   | 400 | kHz   |       |
| Data-in setup time  | t <sup>SU:DAT</sup> | 100 | -   | ns    |       |
| Start condition setup time                                  | t <sup>SU:STA</sup> | 0.6 | -   | μs    | 3     |
| Stop condition setup time                                   | t <sup>SU:STO</sup> | 0.6 | -   | μs    |       |
| WRITE cycle time  | t <sup>WRC</sup>    | -   | 10  | ms    | 4     |

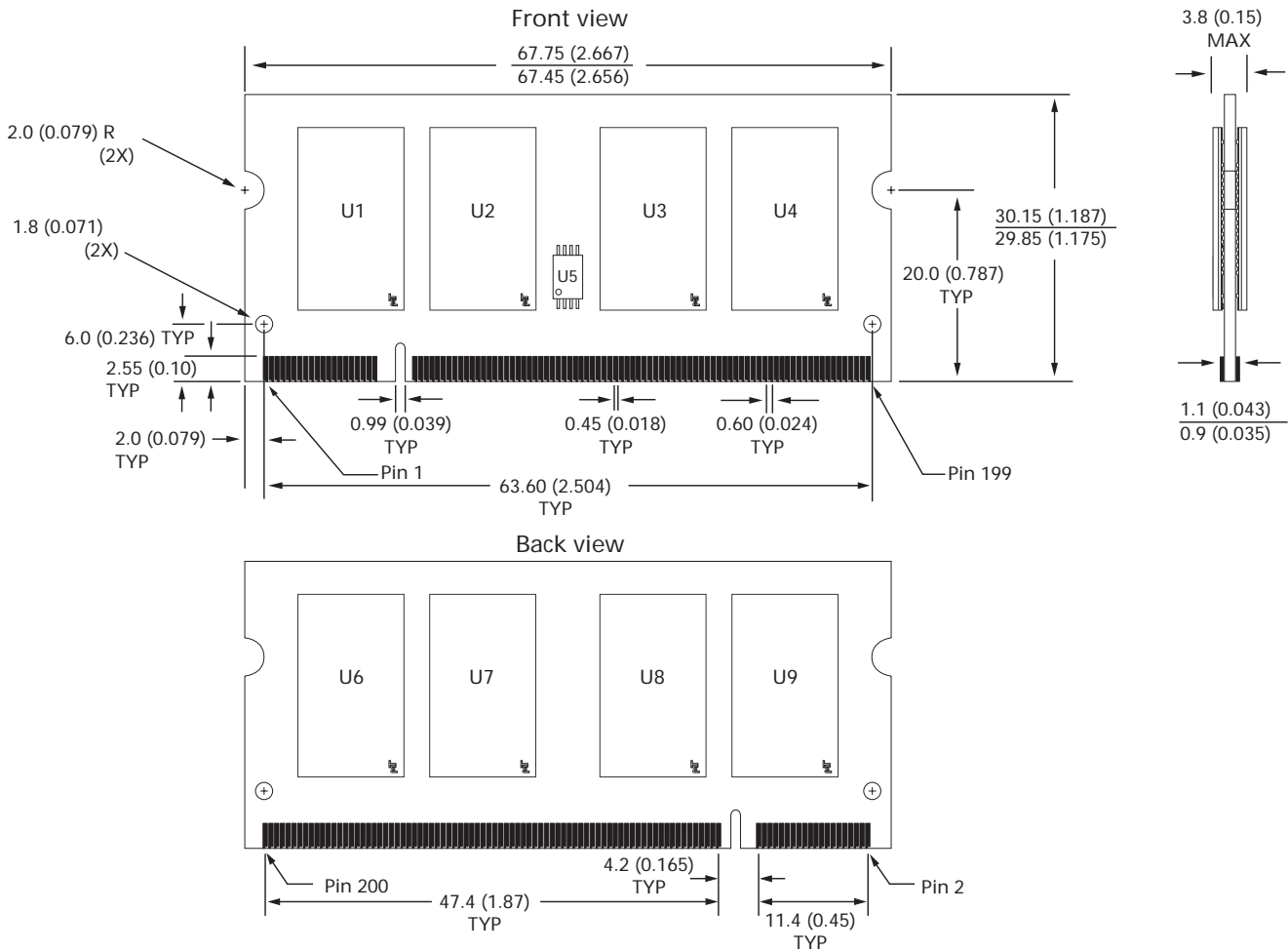
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
  2. This parameter is sampled.
  3. For a restart condition or following a WRITE cycle.
  4. The SPD EEPROM WRITE cycle time (t<sup>WRC</sup>) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

## Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:  
[www.micron.com/SPD](http://www.micron.com/SPD).

## Module Dimensions

Figure 3: 200-Pin DDR2 SODIMM



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or TYP where noted.
  2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.



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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.